IN THE CLAIMS

Please amend the claims to the following.

1. (Currently Amended) A system for maintaining cache coherency in a CMP comprising:
an integrated circuit including
one or more processor cores, wherein the one or more processor cores each include a private cache;
a shared cache separate from the plurality of cores to be shared by the one or more processor cores; and
a ring to connect the one or more processor cores and the shared cache.

2. (Canceled)

3. (Previously Amended) The system of claim 1 wherein the shared cache includes one or more banks.

4. (Original) The system of claim 3 wherein the one or more cache banks is responsible for a subset of a physical address space of the system.

5. (Original) The system of claim 1 wherein the one or more processor cores are write-thru.

6. (Original) The system of claim 5 wherein the one or more processor cores writes data through to the shared cache.

7. (Original) The system of claim 1 wherein the one or more processor cores includes a merge buffer.

8. (Original) The system of claim 7 wherein data is stored in the merge buffer.

9. (Original) The system of claim 8 wherein the merger buffer purges data to the shared cache.

10. (Original) The system of claim 1 wherein the one or more processor cores accesses data from the shared cache.

11. (Original) The system of claim 8 wherein the merger buffer coalesces multiple stores to a same block.

12. (Original) The system of claim 1 wherein the ring is a synchronous, unbuffered bidirectional ring interconnect.

13. (Original) The system of claim 12 wherein a message has a fixed deterministic latency around the ring interconnect.

14. (Currently Amended) An apparatus comprising:

an integrated circuit including: a plurality of cores and a shared memory connected in a ring, the shared cache being separate from the plurality of cores, wherein each of the plurality of cores includes a private cache memory, and wherein the shared memory is accessible by each of the plurality of cores.

15. (Previously Added) The apparatus of claim 14, wherein the plurality of cores and the shared memory are connected in a ring with a synchronous unbuffered bi-directional ring interconnect.

16. (Previously Added) The apparatus of claim 14, wherein the shared memory is a shared cache including a plurality of blocks, and wherein the shared cache is capable of holding each of the plurality of blocks in a cache coherency state.

17. (Previously Added) The apparatus of claim 16, wherein the cache coherency state for each of the plurality of blocks is selected from a group consisting of (1) a not present state, (2) a present and owned by a core of the plurality of cores state, (3) a present, not owned, and custodian is a core of the plurality of cores state, and (4) a present, not owned, and no custodian state.

18. (Currently Amended) An system comprising:

a processor including: a plurality of cores and a shared memory separately coupled ~~together~~ with an unbuffered bi-directional ring interconnect, wherein each of the plurality of cores is associated with a private cache memory, and wherein the shared memory is accessible by each of the plurality of cores; and

a system memory associated with the processor ~~die~~ to hold elements to be stored by the shared memory.

19. (Previously Added) The apparatus of claim 18, wherein the shared memory is a shared cache including a plurality of blocks, and wherein the shared cache is capable of holding each of the plurality of blocks in a cache coherency state.

20. (Previously Added) The apparatus of claim 19, wherein the cache coherency state for each of the plurality of blocks is selected from a group consisting of (1) a not present state, (2) a present and owned by a core of the plurality of cores state, (3) a present, not owned, and custodian is a core of the plurality of cores state, and (4) a present, not owned, and no custodian state.